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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,549	06/20/2003	David John Carr	GB920020011US1	6074

29683 7590 07/11/2006

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EXAMINER	
PEUGH, BRIAN R	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 07/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/600,549	CARR ET AL.	
	Examiner	Art Unit	
	Brian R. Peugh	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19-21* is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This Office Action is in response to applicant's communication filed April 17, 2006 in response to PTO Office Action dated February 10, 2006. The applicant's remarks and amendment to the specification and/or claims were considered with the results that follow.

Claims 1-21 have been presented for examination in this application.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 8 and 16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 8 and 16 recite that the "...interconnect comprises a device driver". It is unclear to the Examiner, in light of Applicant's Specification, how an interconnect (hardware) may be comprised of a device driver (software) without any associated hardware upon which the device driver is to function.

Claim Rejections - 35 USC § 102

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 6, 7, 9-11, 14, 15, 17, and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Kavipurapu (US# 6,584,546).

Regarding claim 1, Kavipurapu teaches **an apparatus for update of cache data in a storage system, the apparatus comprising: a memory for storing data** [Fig. 4; 401a, 401b]; **a cache means for storing data associated with the memory** [col. 4, lines 44-47]; **at least one processor** [Fig. 1] **for preparing change data for updating the cache, the at least one processor comprising circuitry for submitting a request for change to the memory** [Tag search], **receiving a signal from the memory representative of completion of the request for change** [Tag hit response], **and updating the cache with the change data** [write operation] **in response to the signal indicating successful completion of the request for change** [col. 6, line 54 – col. 7,line 19].

Regarding claim 2, Kavipurapu teaches **wherein the data comprises configuration data** [data configured for associative cache scheme; col. 3, lines 3-13].

Regarding claim 3, Kavipurapu teaches **wherein the storage system comprises a disk storage subsystem** [col. 2, lines 57-59; disk drive controller inherently needed for disk drive].

Regarding claim 6, Kavipurapu teaches further comprising **an interconnect**

coupled between the memory and the cache for communicating the request for change, and the signal representative of completion of the request for change [Fig. 6; Search & Hit/Miss bus lines].

Regarding claim 7, Kavipurapu teaches **wherein the interconnect is also arranged to communicate transaction data** [signal data passed on Search & Hit/Miss signal lines may be interpreted as transaction data related to the transaction].

Regarding claim 9, Kavipurapu teaches **a method for update of cache data in a storage system, the method comprising: providing a memory holding data** [Fig. 4; 401a, 401b]; **providing a cache holding data associated with the memory** [col. 4, lines 44-47]; **preparing change** [new or updated] **data for updating the cache; submitting a request for change to the memory** [Tag search]; **receiving a signal from the memory representative of completion of the request for change** [Tag hit response]; **and updating the cache means with the change data in response to the signal indicating successful completion of the request for change** [col. 6, line 54 – col. 7,line 19].

Regarding claim 10, Kavipurapu teaches **wherein the data comprises configuration data** [data configured for associative cache scheme; col. 3, lines 3-13].

Regarding claim 11, Kavipurapu teaches **wherein the storage system comprises a disk storage subsystem** [col. 2, lines 57-59; disk drive controller inherently needed for disk drive].

Regarding claim 14, Kavipurapu teaches further comprising **an interconnect**

coupled between the memory and the cache for communicating the request for change, and the signal representative of completion of the request for change [Fig. 6; Search & Hit/Miss bus lines].

Regarding claim 15, Kavipurapu teaches **wherein the interconnect is also arranged to communicate transaction data** [signal data passed on Search & Hit/Miss signal lines may be interpreted as transaction data related to the transaction].

Regarding claim 17, Kavipurapu teaches **a computer program storage device readable by a machine and comprising executable computer program instructions for update of a cache in a storage system, the storage system comprising a memory holding data and a cache holding data associated with the memory, the instructions for performing the method of: preparing change** [new or updated] **data for updating the cache** [col. 4, lines 44-47]; **submitting a request for change to the memory** [Fig. 4; 401a, 401b; Tag search]; **receiving a signal from the memory representative of completion of the request for change** [Tag hit response]; **and updating the cache means with the change data in response to the signal indicating successful completion of the request for change** [col. 6, line 54 – col. 7,line 19]. The limitations directed towards executable program instructions has not been given patentable weight due to the fact that the limitations are only found within the claims preamble and not within the body of the claim.

Regarding claim 18, Kavipurapu teaches **an apparatus for update of cache data in a storage system, the apparatus comprising: providing a memory holding data** [Fig. 4; 401a, 401b]; **providing a cache holding data associated with the**

memory [col. 4, lines 44-47]; **preparing change** [new or updated] **data for updating the cache; submitting a request for change to the memory** [Tag search]; **receiving a signal from the memory representative of completion of the request for change** [Tag hit response]; **and updating the cache means with the change data in response to the signal indicating successful completion of the request for change** [col. 6, line 54 – col. 7,line 19].

Claims 1, 3-5, 9, 11-13, 17, and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Hubis (US# 6,321,298).

Regarding claim 1, Hubis teaches **an apparatus for update of cache data in a storage system, the apparatus comprising: a memory for storing data** [1st receiving controller write cache (118)]; **a cache means for storing data associated with the memory** [2nd receiving controller write cache (118)]; **at least one processor** [processor interpreted as sending controller (104); Fig. 6; see also Fig. 3] **for preparing change data for updating the cache, the at least one processor comprising circuitry for submitting a request for change to the memory** [col. 4, lines 13-20], **receiving a signal from the memory representative of completion of the request for change** [col. 4, lines 20-22], **and updating the cache with the change data in response to the signal indicating successful completion of the request for change** [col. 4, lines 27-31; Hubis indicates that the multiple updating *can* occur simultaneously, which inherently teaches that the updates may be performed serially and separate from each other].

Regarding claim 3, Hubis teaches **wherein the storage system comprises a disk storage subsystem** [col. 3, liens 2-15].

Regarding claim 4, Hubis teaches **wherein the memory is comprised in a disk adapter** [disk 'adapter' interpreted as a disk controller 'adapted' to perform operations on the disk; 1st memory (cache) within RAID controller 104; Fig. 3].

Regarding claim 5, Hubis teaches **wherein the memory is comprised in a disk controller** [1st memory (cache) within RAID controller 104; Fig. 3].

Regarding claim 9, Hubis teaches **a method for update of cache data in a storage system, the method comprising: providing a memory holding data** [1st receiving controller write cache (118)]; **providing a cache holding data associated with the memory** [2nd receiving controller write cache (118)]; **preparing change data for updating the cache; submitting a request for change to the memory** [col. 4, lines 13-20]; **receiving a signal from the memory representative of completion of the request for change** [col. 4, lines 20-22], **and updating the cache means with the change data in response to the signal indicating successful completion of the request for change** [col. 4, lines 27-31; Hubis indicates that the multiple updating *can* occur simultaneously, which inherently teaches that the updates may be performed serially and separate from each other].

Regarding claim 11, Hubis teaches **wherein the storage system comprises a disk storage subsystem** [col. 3, liens 2-15].

Regarding claim 12, Hubis teaches **wherein the memory is comprised in a disk adapter** [disk 'adapter' interpreted as a disk controller 'adapted' to perform operations on the disk; 1st memory (cache) within RAID controller 104; Fig. 3].

Regarding claim 13, Hubis teaches **wherein the memory is comprised in a disk controller** [1st memory (cache) within RAID controller 104; Fig. 3].

Regarding claim 17, Hubis teaches **a computer program storage device readable by a machine and comprising executable computer program instructions for update of a cache in a storage system, the storage system comprising a memory holding data and a cache holding data associated with the memory, the instructions for performing the method of: preparing change data for updating the cache** [col. 4, lines 13-20]; **submitting a request for change to the memory; receiving a signal from the memory representative of completion of the request for change** [col. 4, lines 20-22], **and updating the cache means with the change data in response to the signal indicating successful completion of the request for change** [col. 4, lines 27-31; Hubis indicates that the multiple updating *can* occur simultaneously, which inherently teaches that the updates may be performed serially and separate from each other. The limitations directed towards executable program instructions has not been given patentable weight due to the fact that the limitations are only found within the claims preamble and not within the body of the claim.

Regarding claim 18, Hubis teaches **an apparatus for update of cache data in a storage system, the apparatus comprising: providing a memory holding data** [1st

receiving controller write cache (118)]**providing a cache holding data associated with the memory** [2nd receiving controller write cache (118)];; **preparing change** [new or updated] **data for updating the cache; submitting a request for change to the memory** [col. 4, lines 13-20]; **receiving a signal from the memory representative of completion of the request for change** [col. 4, lines 20-22], **and updating the cache means with the change data in response to the signal indicating successful completion of the request for change** [col. 4, lines 27-31; Hubis indicates that the multiple updating *can* occur simultaneously, which inherently teaches that the updates may be performed serially and separate from each other.].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kavipurapu (US# 6,584,546) as applied to claims 1-3, 6, 7, 9-11, 14, 15, 17, and 18 above, and further in view of Tanenbaum. The following rejection is made in light of the aforementioned 35 U.S.C.,. 112 second paragraph rejection.

The difference between the claimed subject matter of claims 8 and 16 and that of Kavipurapu is that the claims recite that the interconnect comprises a device driver.

Tanenbaum teaches that hardware and software are logically equivalent [page 11, para. 1-3]. Therefore it would have been obvious to one of ordinary skill in the art having the teachings of Kavipurapu before him at the time the invention was made to modify the caching system of Kavipurapu to include the software device driver of Tanenbaum because then benefits in speed, cost, and reliability could be realized [page 11, para. 3].

Allowable Subject Matter

Claims 19-21 are allowed over the prior art of record.

Response to Arguments

Applicant's arguments filed 04/17/06 have been fully considered but they are not persuasive.

Regarding Applicant's arguments of page seven, paragraph two in reference to the 35 U.S.C., second paragraph rejections, the Examiner acknowledges the cited Specification references. However, claim 8 must be read in light of parent claim 6 which requires an interconnect be coupled between the memory and the cache. Thus, claim 8 requires that the interconnect be comprised of hardware in order to couple to the memory and cache.

Regarding Applicant's arguments on page 10 that the Kavipurapu reference does not teach at least claim 1, the Examiner disagrees with Applicant's assertion that a tag search is not a submission of a request for a change to memory. The tag search is but a portion of the write operation (request for a change to memory). The Kavipurapu

refrences also teaches the receiving step in that a tag hit leads to a tag overwrite, such that the receiving limitation is not limited by what component receives the signal. The controller receives the tag hit signal in order to process the overwrite of the tag that matches the same tag in the tag directory and sets the valid bit [col. 6, lines 51-58].

Regarding claims 2 and 10, the Examiner would like to point out that Kavipurapu teaches the claimed subject matter via not only the fully associative, but also the set associate cache systems [col.3, lines 8-12.

Regarding Applicant's assertion that the Kavipurapu reference does not teach claims 4 and 12, the Examiner agrees because the Kavipurapu reference was not used to teach claims 4 and 12.

Regarding claims 7 and 15, given the broadest reasonable interpretation, instructions and data read upon the "transaction data" as claimed, because the instruction is part of the transaction the leads to the acquiring or writing of data, also part of the write operation (transaction).

Regarding Applicant's assertion on page 12 that "a command is not a request", Hubis teaches a command for writing data into a cache, which when given a broad, reasonable interpretation, would read upon the "request" as claimed. The "request" as claimed may be broadly interpreted as a command or instruction.

Further, in reference to the arguments of page 13, the Examiner has previously asserted that a request for change to the memory may be interpreted as an access or write access to cache, both taught by Kavipurapu and Hubis. Also, the Examiner has shown that the valid bit in reference to a write operation. The Examiner is unclear,

however, as to Applicant's assertion that "...the valid bit concerns a cache line and not data that is associated with memory" (lines 11-12) in light of "A valid bit appears to hold a value that is used internally by the memory..." (line 20).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian R. Peugh whose telephone number is (571) 272-4199. The examiner can normally be reached on Monday-Thursday from 7:00am to 4:30pm. The examiner can also be reached on alternate Friday's from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks, can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian R. Peugh
Primary Examiner
July 6, 2006